WE CLAIM:

1. A synchronization (sync) signal detector comprising:

a) a sync signal generator for generating a reference sync signal;

b) a sampler connected to the sync signal generator;

c) a waveform correlator connected to the sampler, the waveform correlator receiving a input signal; and

d) a peak detector connected to the waveform correlator and the sampler.

2. The sync signal detector of claim 1 further comprising a synchronization information calculator connected to the waveform correlator and the peak detector, the synchronization information calculator providing data to one or more components external to the synchronization signal detector.

3. The sync signal detector of claim 1, further comprising:

a phase calculator connected to receive a frequency modulated input signal; and

a frequency modulation (FM) demodulator connected to the phase calculator and to the waveform correlator and configured to provide a frequency demodulated output signal as the input signal to the waveform correlator.

4. The sync signal detector of claim 3, implemented in a communication signal receiver.

5. The sync signal detector of claim 4, further comprising a synchronization information calculator connected to the waveform correlator and the peak detector, the synchronization information calculator providing data to one or more components of the receiver external to the sync signal detector.

6. The sync signal detector of claim 5, wherein the synchronization information comprises a modulation index.

7. The sync signal detector of claim 5, wherein the synchronization information comprises a frequency offset.

8. The sync signal detector of claim 1, wherein the waveform correlator and the peak detector are implemented in a digital signal processor (DSP).

9. The sync signal detector of claim 1, implemented in a communication device selected from the group consisting of wired and wireless modems, hand-held communication devices, personal digital assistants (PDAs) with communication functions, cellular telephones, one-way pagers and two-way pagers.

10. A process for detecting a synchronization (sync) signal within an input signal, said process comprising the steps of:

a) generating a version of the sync signal;

b) correlating the sync signal with the input signal to generate a correlation signal;

c) detecting a correlation peak in the correlation signal;

d) estimating a timing offset based on the correlation peak for use by step a);

e) repeating step a) to generate a shifted version of the sync signal using the timing offset estimated in step d); and

f) further processing the input signal based on the shifted version of the sync signal until the end of the input signal.

11. The process of claim 10 further comprising the step between steps e) and f) of determining and outputting synchronization information.

12. The process of claim 10 wherein step a) is selected from the set consisting of:

i) generating the sync signal utilizing a known timing offset;

ii) generating the sync signal and then shifting sampling points at which the sync signal is sampled by a known timing offset; and

iii) generating the sync signal utilizing a known timing offset and then sampling the sync signal.

13. The process of claim 10, wherein the input signal is a frequency modulated input signal, the process further comprising the steps of:

calculating the phase of the input signal; and

frequency demodulating a resultant signal from the step of calculating the phase to produce a frequency demodulated signal for use by step b).

14. The process of claim 13 further comprising the step between steps e) and f) of determining and outputting synchronization information.

15. The process of claim 14 wherein said synchronization information comprises a frequency offset.

16. The process of claim 14 wherein said synchronization information comprises a modulation index.

17. A synchronization (sync) signal detector comprising:

a) means for generating an internal sync signal;

b) means for sampling said internal sync signal, the means for sampling operatively connected to the means for generating;

c) means for correlating a waveform, the means for correlating operatively connected to the means for sampling, the means for correlating receiving a input signal; and

d) means for detecting a peak, the means for detecting a peak operatively connected to the means for correlating and the means for sampling.

18. A method for detecting a data pattern in an input signal, said method comprising the steps of:

a) matching the data pattern to a known sync pattern using waveform correlation;

b) shifting the known sync pattern by a timing offset determined from the waveform correlation to create a shifted sync pattern; and

c) utilizing the shifted sync pattern to further process the input signal.

19. The method of claim 18 further comprising the step d) of generating synchronization information.

20. The method of claim 19 wherein the synchronization information comprises a frequency offset.

21. The method of claim 19 wherein the synchronization information comprises a modulation index.

22. The method of claim 19 wherein the step of generating synchronization information comprises the steps of:

calculating a modulation index (g) of the input signal using the shifted sync signal, as $g = \frac{\sum_i r_i * t_i - \frac{1}{N}\sum_i r_i \sum_i t_i}{\sum_i t_i^2 - \frac{1}{N}\left(\sum_i t_i^2\right)}$; and

calculating a frequency offset (dc) of the input signal using the shifted sync signal, as $dc = \frac{1}{N}\left(\sum_i r_i - g\sum_i t_i\right)$,

where r_i denotes digital samples of the data pattern, t_i denotes digital samples of the shifted sync signal, and i = 1,2,...N are indexes of the samples of the input signal and the shifted sync signal.

23. The method of claim 22, further comprising the steps of:

calculating an amount of noise (E) present in the received signal, using the shifted sync signal, as $E = \sum_i (r_i - gt_i - dc)^2$;

comparing the calculated noise E to a threshold T to determine whether or not the received signal samples r_i represent a valid sync signal; and

performing step c) only if it is determined that the received signal samples represent a valid sync signal.

24. The method of claim 18, wherein step b) comprises shifting sampling points within said known sync pattern by the timing offset determined from the waveform correlation to create the shifted sync pattern.

25. A computer readable medium containing instructions for implementing a method for detecting a data pattern in an input signal, the method comprising the steps of:

a) matching the data pattern to a known sync pattern using waveform correlation;

b) shifting the known sync pattern by a timing offset determined from the waveform correlation to create a shifted sync pattern; and

c) utilizing the shifted sync pattern to further process the input signal.

26. The medium of claim 25, implemented in a digital signal processor (DSP).

27. A wireless communication device comprising:

a transceiver configured to transmit and receive communication signals; and

a digital signal processor (DSP) operatively coupled to the transceiver, the DSP comprising computer software code for detecting a data pattern in a communication signal, by performing the functions of:

a) matching the data pattern to a known sync pattern using waveform correlation;

b) shifting the known sync pattern by a timing offset determined from the waveform correlation to create a shifted sync pattern; and

c) utilizing the shifted sync pattern to further process the communication signal.

28. The device of claim 27, wherein the device is selected from the group consisting of wired and wireless modems, hand-held communication devices, personal digital

assistants (PDAs) with communication functions, cellular telephones, one-way pagers and two-way pagers.